

**Al Mansoura University**

**Faculty of Engineering**

**Electronics and Communications Dept.**

**2<sup>nd</sup> Year Students**

**Logic Circuit 2**

**First Semester 2013**

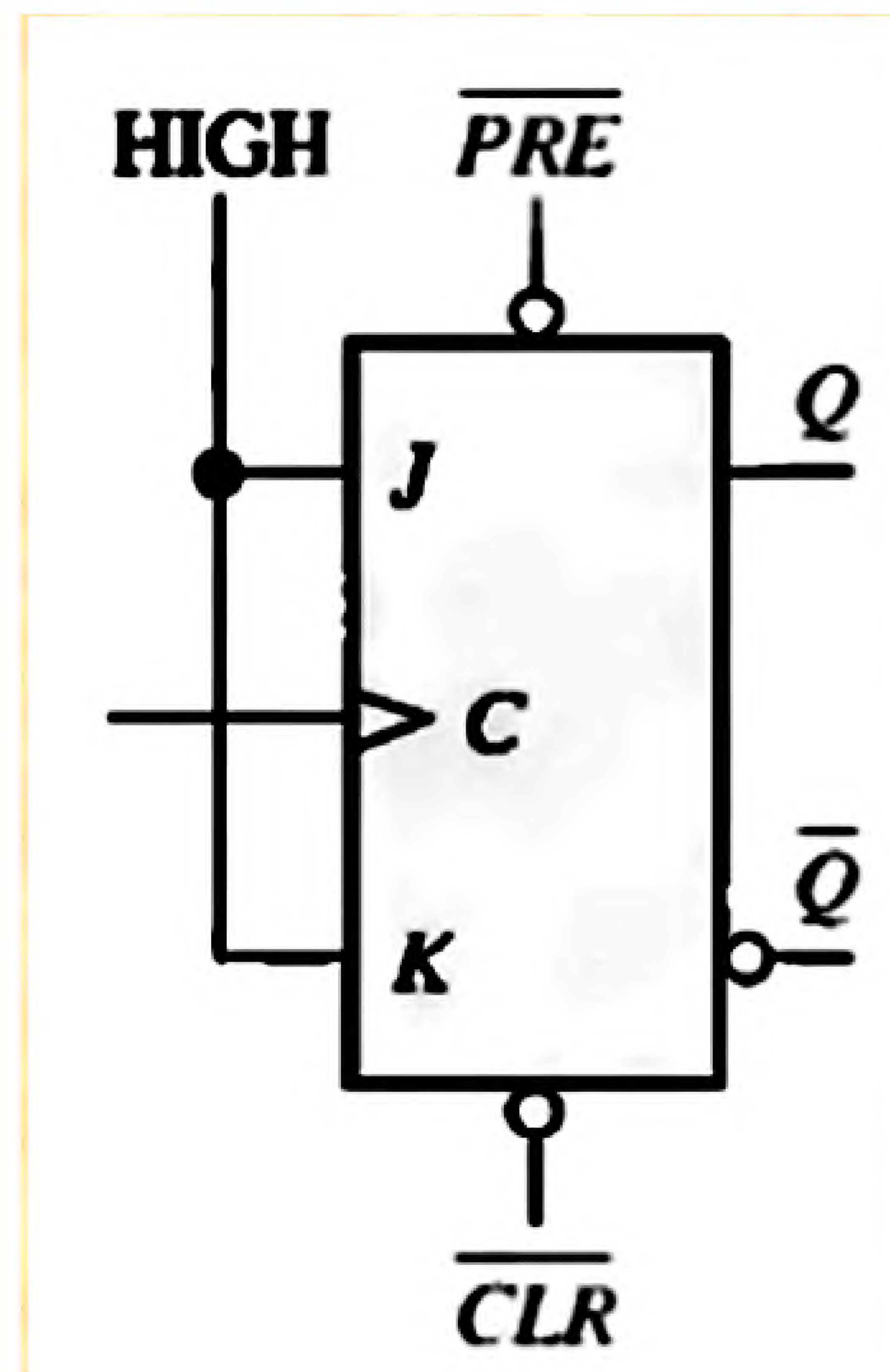
**Prepared By: Dr. Muhammad Morsy**

**Chapter 1: Latches**

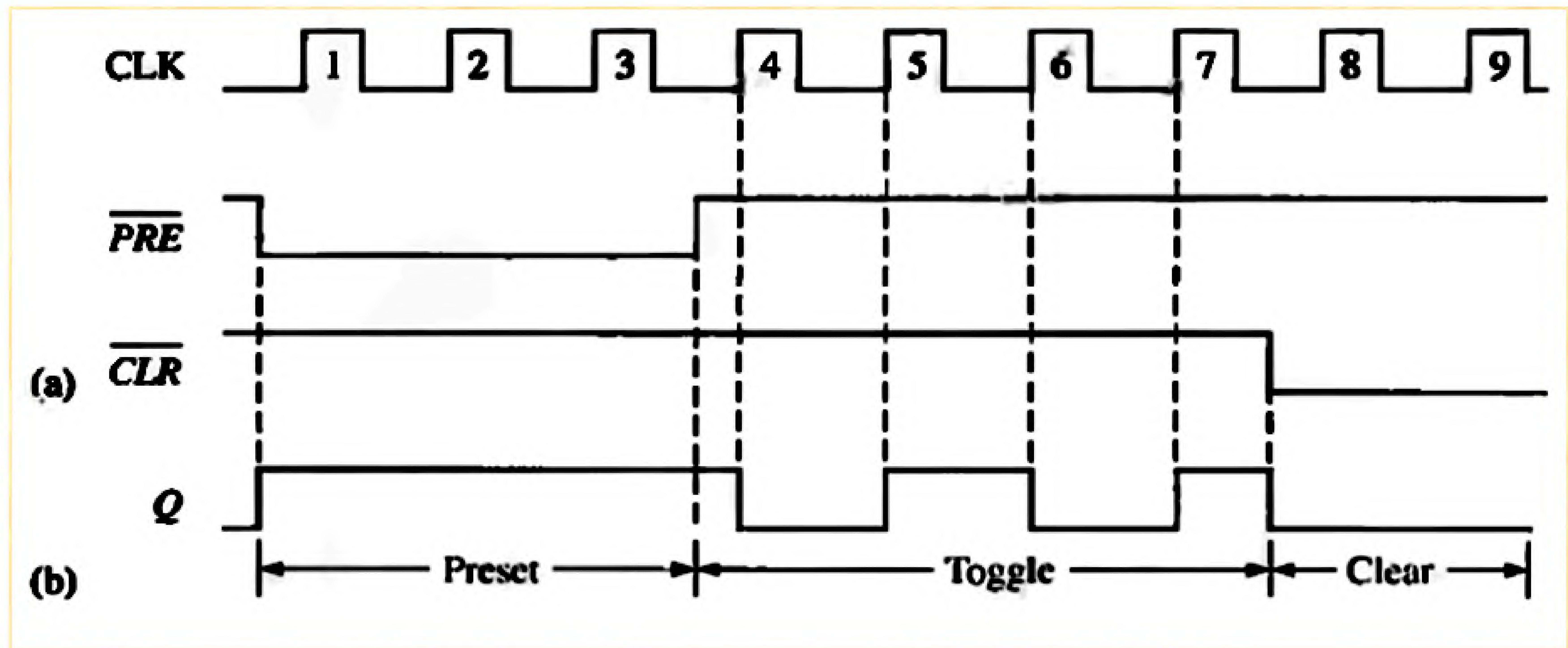
**Lecture No. 3**



**Example 1.8:** For the positive edge-triggered J-K flip-flop with **preset** and **clear** inputs shown in the Figure, determine the Q output for the inputs shown in the timing diagram in part (a) if Q is initially **LOW**.









### **Solution:**

1. During clock pulses 1,2, and 3, the **preset** (PRE) is **LOW**, keeping the flip-flop **SET** regardless of the **synchronous** and **K** inputs.
2. For clock pulse 4,5, 6, and 7, **toggle operation** occurs because **J** is **HIGH**, **K** is **HIGH**, and both **PRE** and **CLR** are **HIGH**.
3. For clock pulses 8 and 9, the **clear** (CLR) input is **LOW**, keeping the flip-flop **RESET** regardless of the **synchronous** inputs.



### 1.10- Flip-flop Operating Characteristics.

- ✓ The **performance**, **operating** requirements, and **limitations** of flip-flops are **specified** by several **operating characteristics** or **parameters** found on the **data sheet** for the device.
- ✓ Generally, the specifications are applicable to all **CMOS** and **TTL** flip-flops.



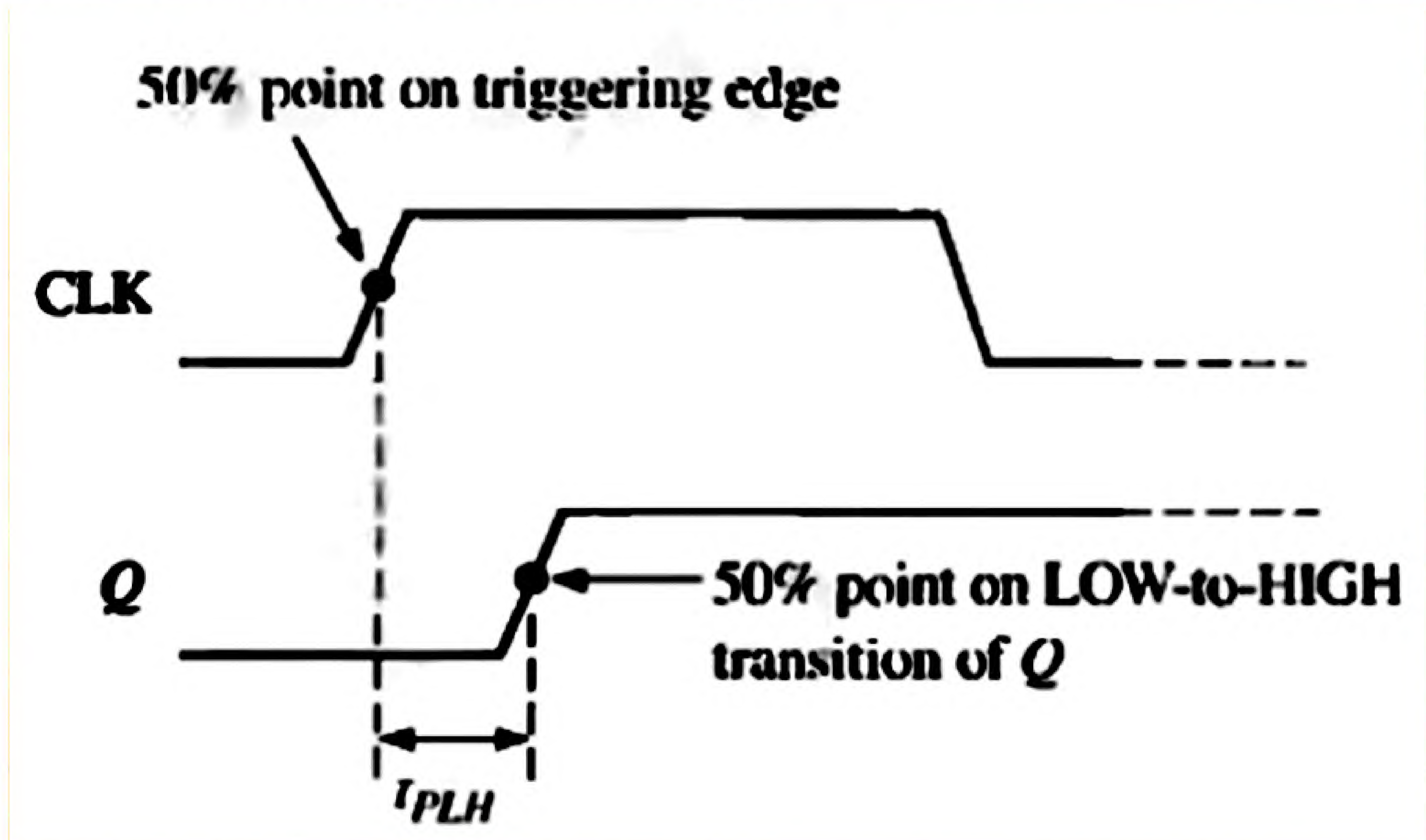
### 1.10.1-Propagation Delay Times.

- ✓ A **propagation delay time** is the interval of time required after an **input signal** has been **applied** for the resulting output change to occur.
- ✓ **Four categories** of propagation delay times are important in the operation of a flip-flop:



### (1)- Propagation delay, $t_{PLH}$

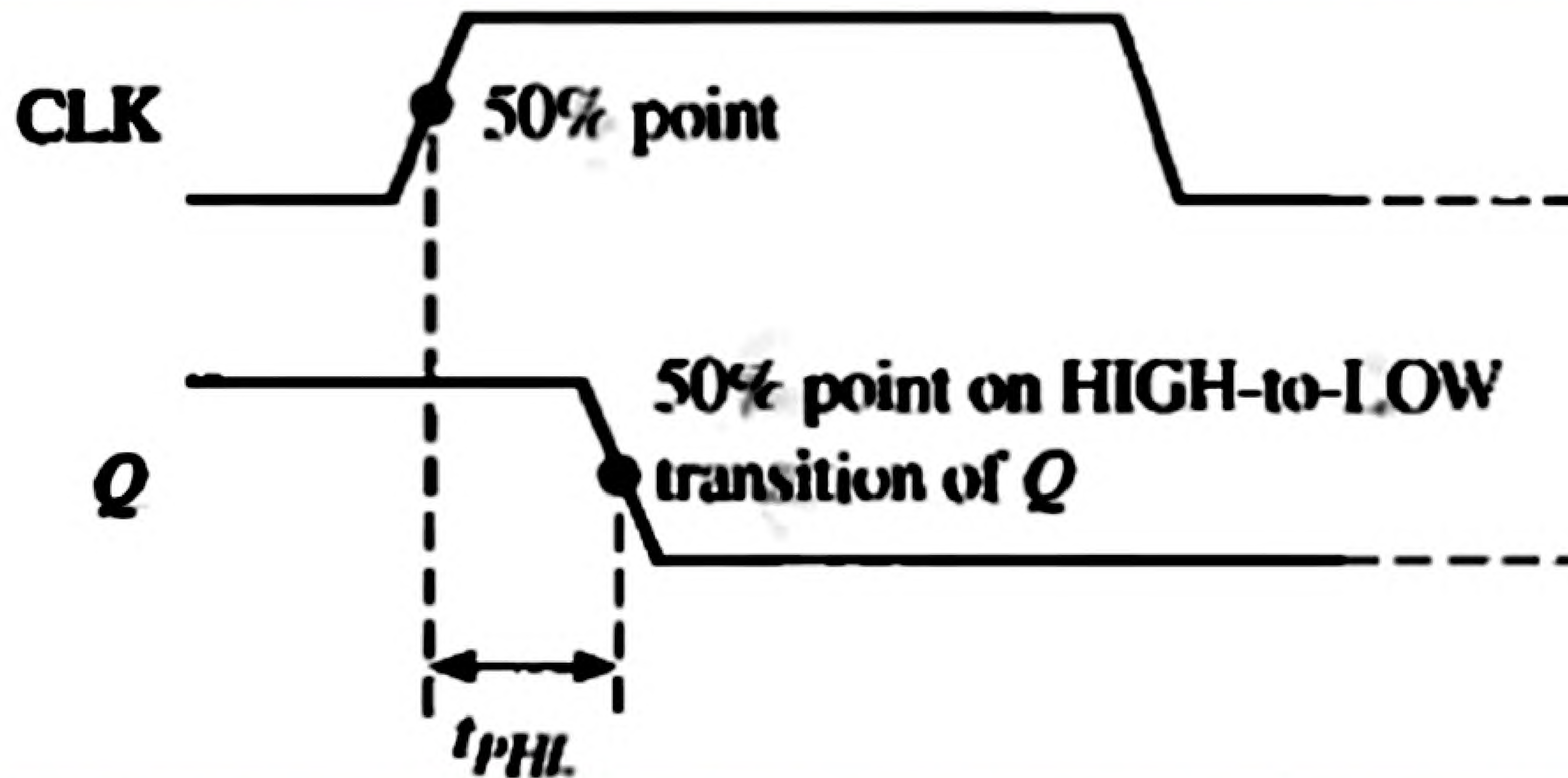
- ✓ As measured from the **triggering edge** of the clock pulse to the **LOW-to-HIGH** transition of the output. This delay is illustrated in Figure 1-15 (a).





## (2)- Propagation delay, $t_{PHL}$

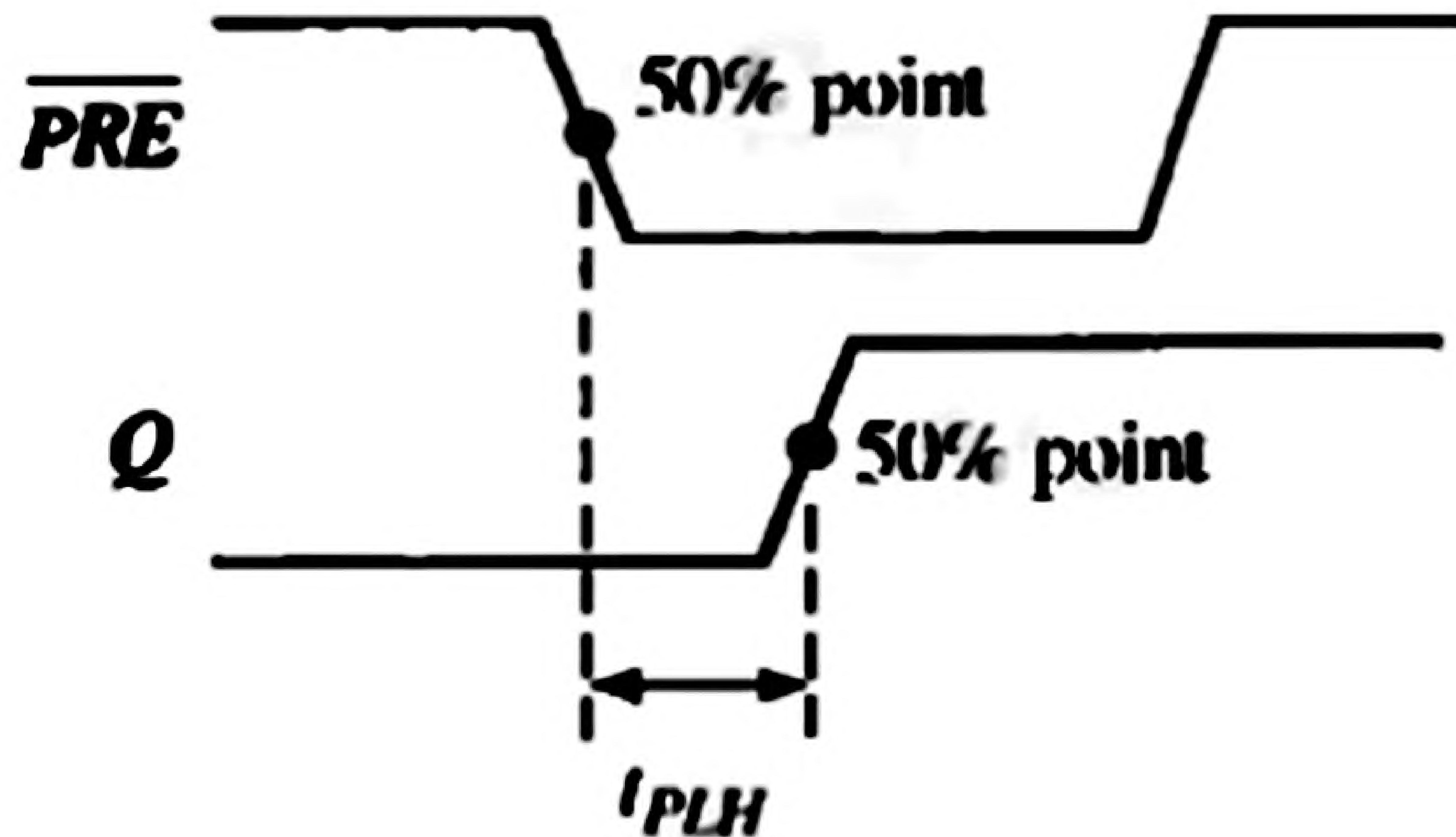
- ✓ As measured from the **triggering edge** of the clock pulse to the **HIGH-to-LOW** transition of the output. This delay is illustrated in Figure 1-15(b).





### (3)- Propagation delay, $t_{PLH}$

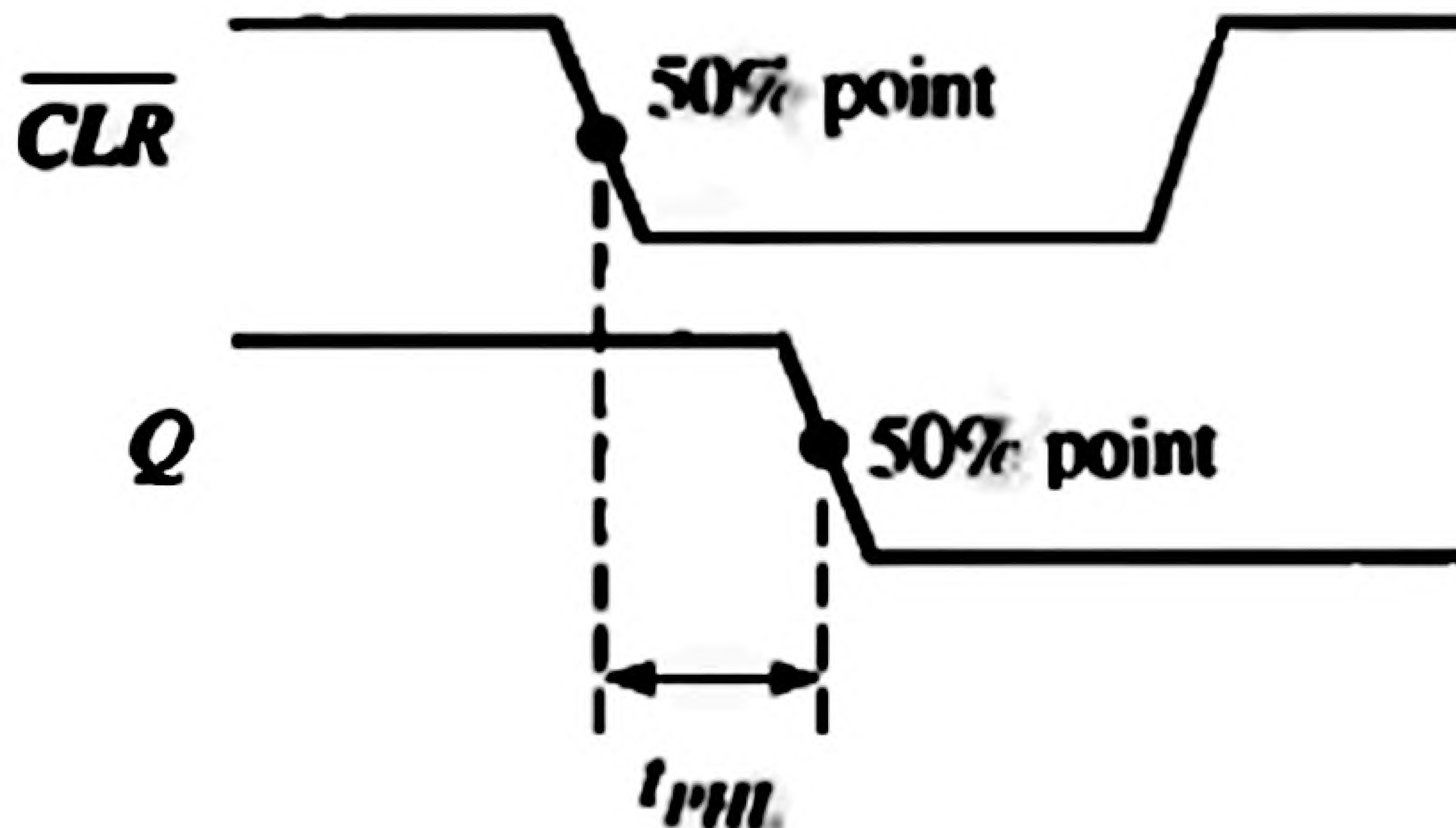
- ✓ As measured from the **leading edge** of the **PRESET** input to the **LOW-to-HIGH** transition of the output. This delay is illustrated in Figure 1.16 (a) for an active-LOW preset input.





#### (4)- Propagation delay, $t_{PHL}$

- ✓ As measured from the **leading edge** of the **CLEAR** input to the **HIGH-to-LOW** transition of the output. This delay is illustrated in Figure 1.16(b) for an active-LOW clear input.

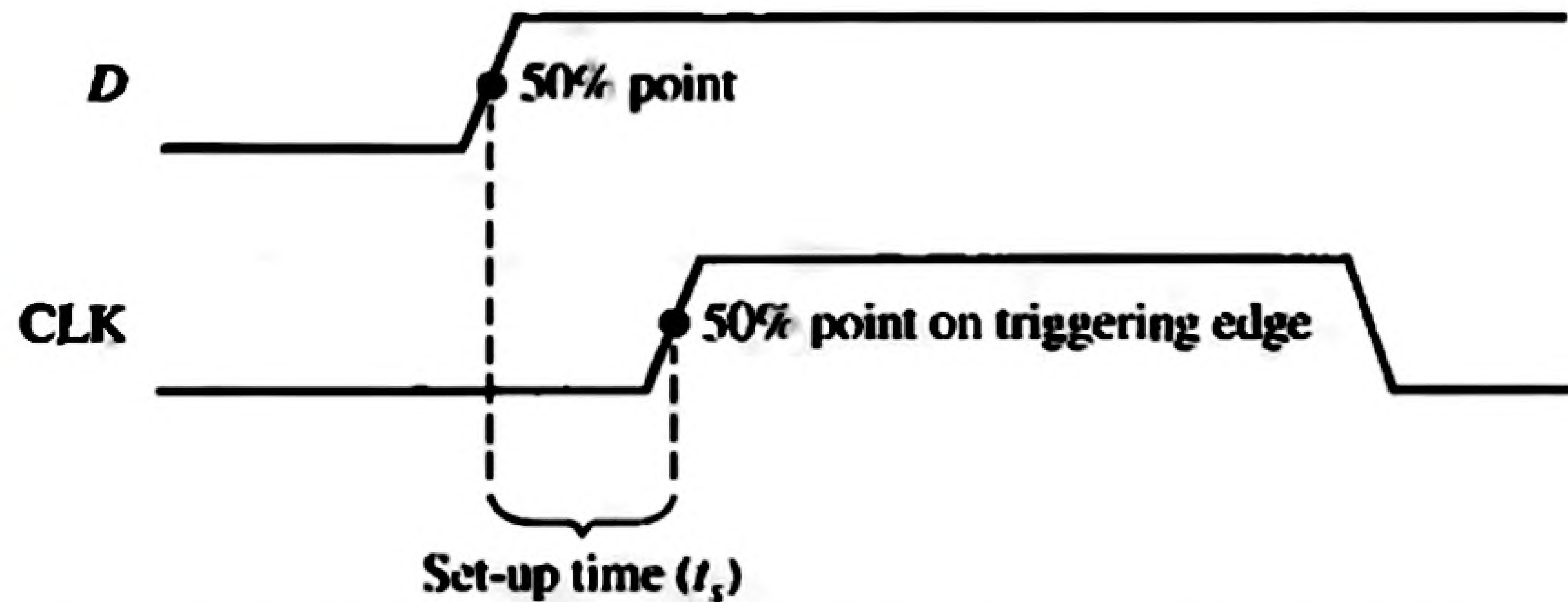




### 1.10-2-Set-up Time.

- ✓ The **set-up** time  $t_s$  is the **minimum interval** required for the logic levels to be **maintained constantly** on the inputs (J and K, or S and R, or D) **prior** to the **triggering** edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. This interval is illustrated in Figure 1.17 for a D flip-flop.





**Figure 1.17** Set-up time,  $t_s$



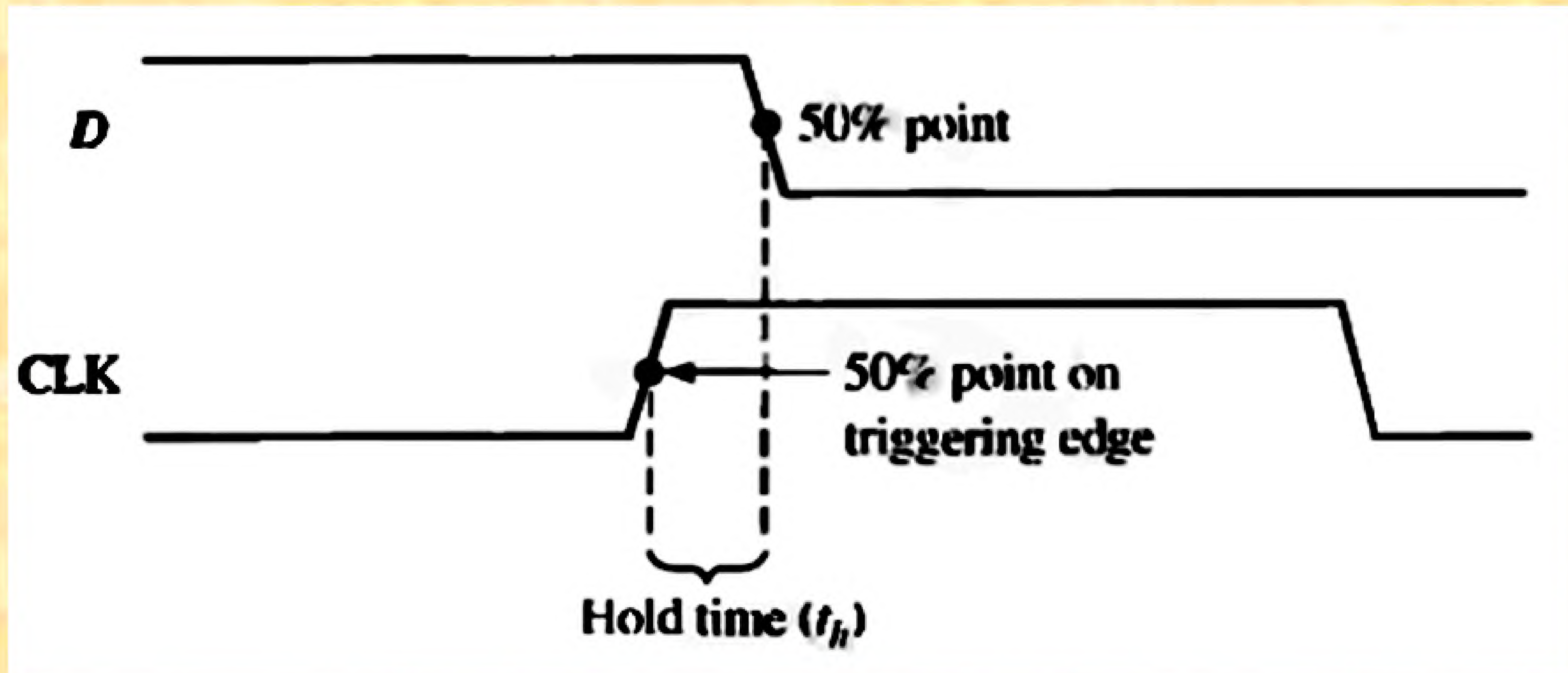
- ✓ The **logic level** must be **present** on the D input for a time **equal** to or **greater** than  $t_s$ , before the triggering edge of the clock pulse for reliable data entry.

### 1.10-3-Hold Time.

- ✓ The **hold time**  $t_h$  is the **minimum interval** required for the logic levels to **remain** on the inputs **after** the **triggering edge** of the clock pulse in order for the levels to be reliably



clocked into the flip-flop. This is illustrated in Figure 1.18 for a D flip-flop.



**Figure 1.18** Hold time  $t_h$



- ✓ The **logic level** must **remain** on the D input for a time **equal** to or **greater** than  $t_h$  after the **triggering edge** of the clock pulse for reliable data entry.

#### 1.10.4-Maximum Clock Frequency.

- ✓ The **maximum clock frequency**  $f_{\max}$  is the **highest rate** at which a flip-flop can be **reliably triggered**.
- ✓ At clock frequencies **above** the **maximum**, the flip-flop would be **unable** to **respond** quickly enough, and its operation would be impaired.



### 1.10.5- Pulse Widths.

- ✓ **Minimum** pulse widths  $t_w$  for **reliable** operation are usually specified by the **manufacturer** for the clock, **PRESER**, and **CLEAR** inputs.
- ✓ Typically, the clock is specified by its minimum HIGH time and its minimum LOW time.

### 1.10.6- Power Dissipation.

- ✓ The power dissipation of any digital circuit is the **total power** consumption of the device. For example, if the flip-



flop operates on a **+ 5 V dc source** and draws **5 mA** of current, the **power dissipation** is:

$$P = V_{CC} \times I_{CC} = 5 \text{ V} \times 5 \text{ mA} = 25 \text{ mW}$$

- ✓ The **power dissipation** is very important in most applications in which the **capacity** of the **dc supply** is a concern.
- ✓ As an example, let's **assume that** you have a **digital system** that requires a total of **ten flip-flops**, and each flip-flop dissipates **25 mW** of power. The **total power** requirement is:



$$P_T = 10 \times 25 \text{ mW} = 250 \text{ mW} = \mathbf{0.25W}$$

- ✓ This tells you the output capacity required of the dc supply.
- ✓ If the flip-flops operate on **+5 V dc**, then the **amount** of **current** that the supply must provide is:

$$I = \frac{250 \text{ mW}}{5 \text{ v}} = 50 \text{ mA}$$

- ✓ You must use a **+5 V dc** supply that is capable of providing at least **50 mA** of current.



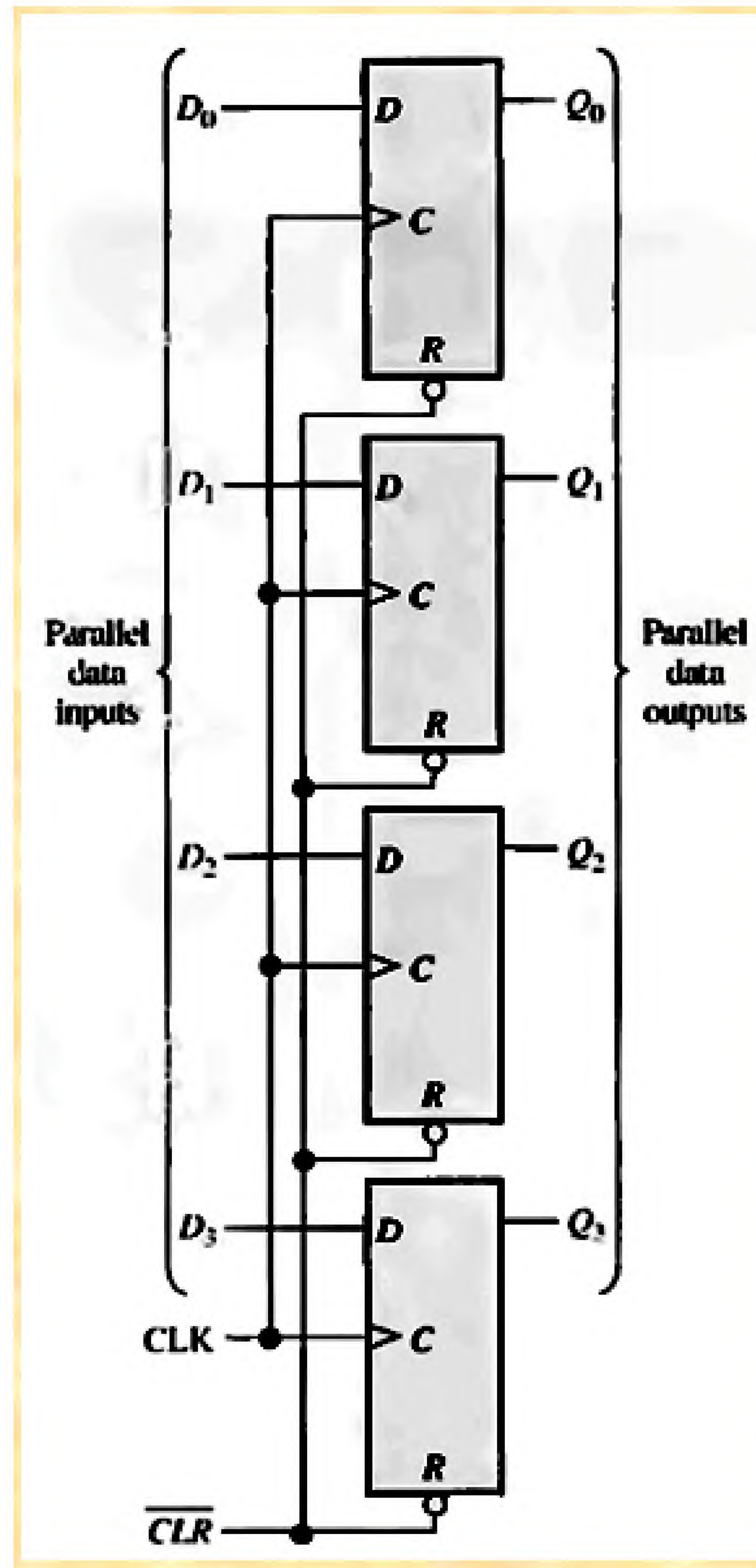
### 1.11- Flip-flop Applications.

- ✓ In this section, **three general** applications of flip-flops are discussed to give you an idea of how they can be used.

#### 1.11.1- Parallel Data Storage.

- ✓ A **common requirement** in digital systems is to **store several** bits of data from **parallel lines** simultaneously in a group of flip-flops.
- ✓ This operation is illustrated in Figure 1.19 (a) using four flip-flops.

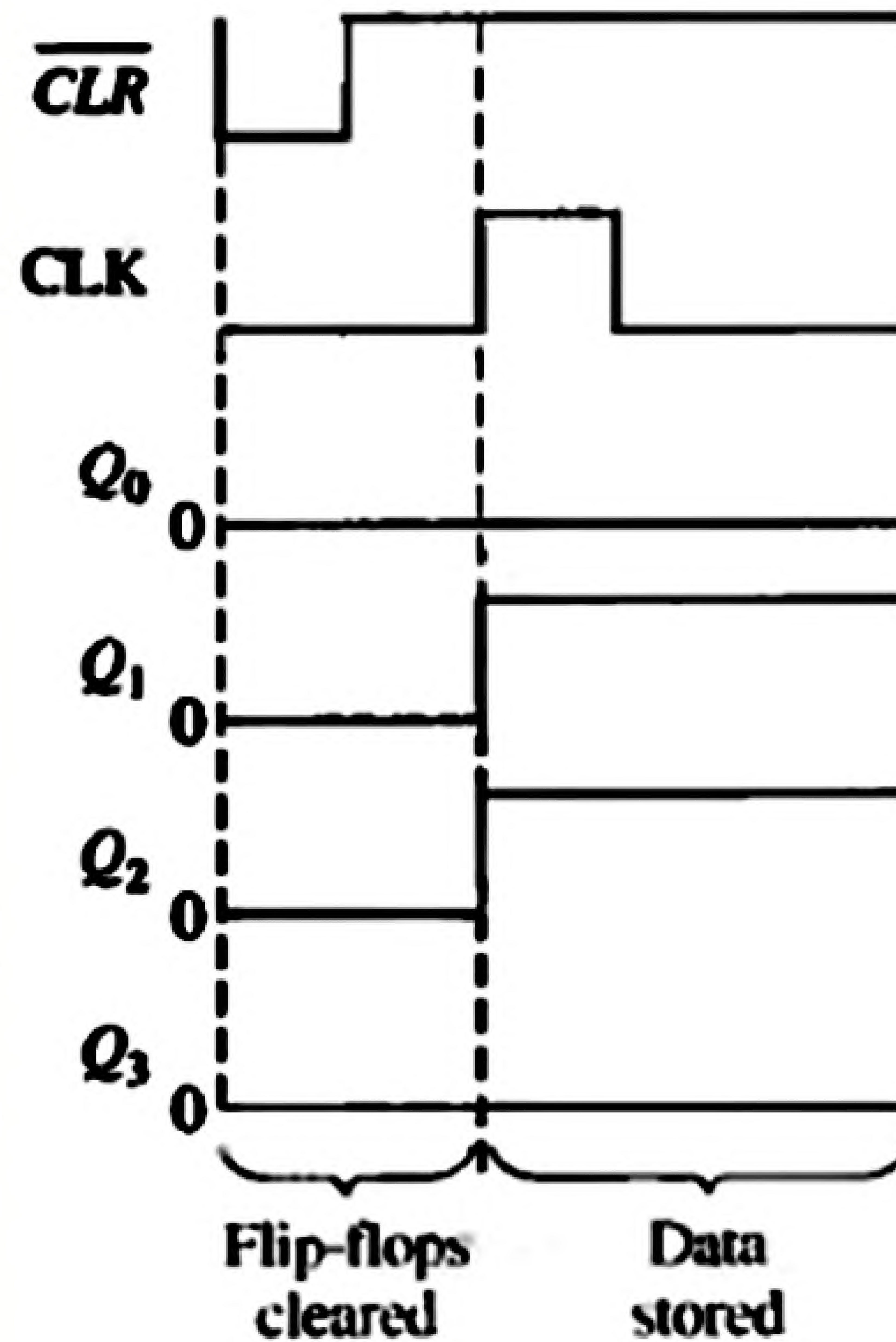
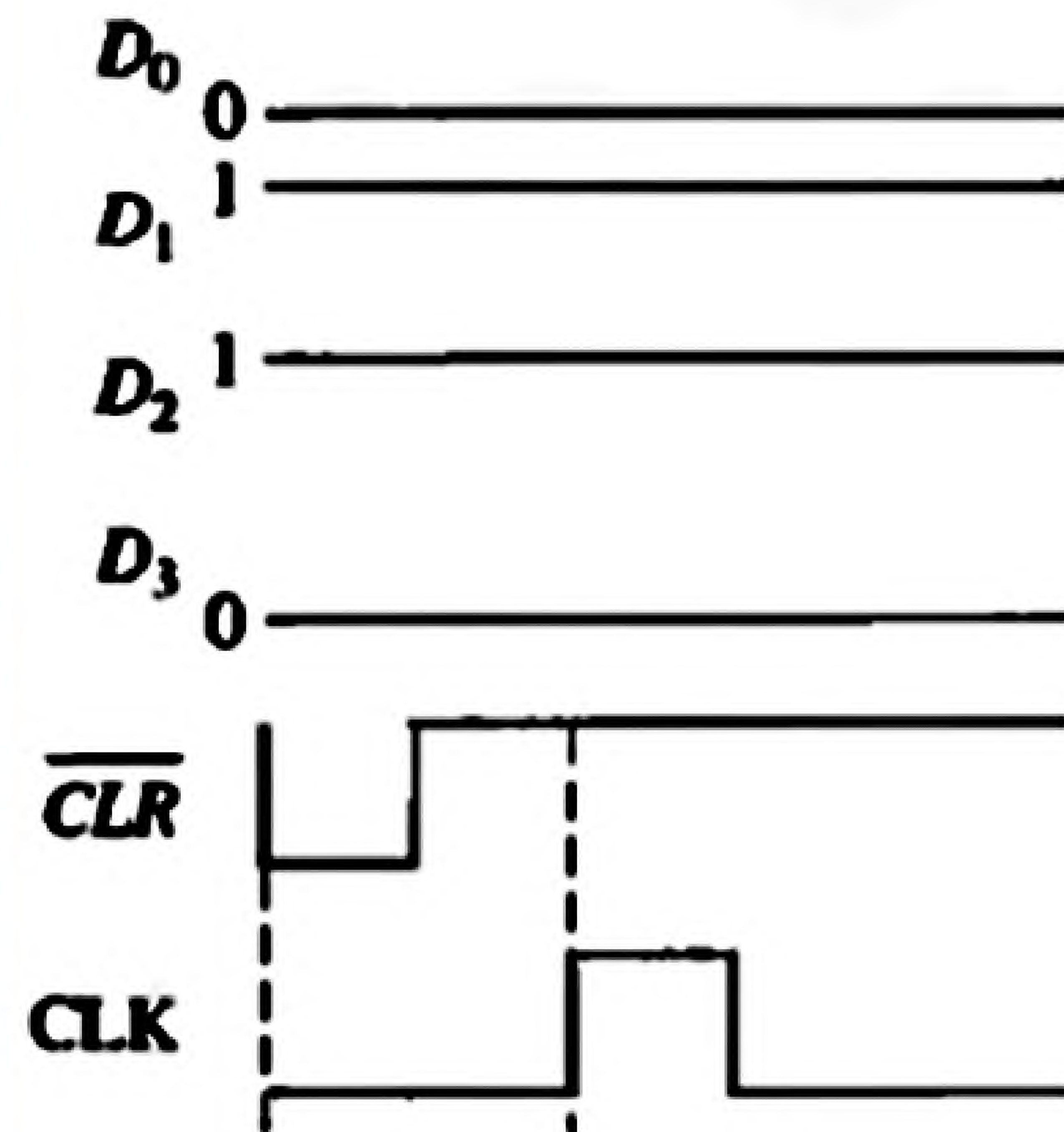






- ✓ Each of the **four parallel** data lines is **connected** to the D input of a flip-flop.
- ✓ The **clock inputs** of the flip-flops are **connected together**, so that each flip-flop is **triggered** by the **same** clock pulse.
- ✓ In this example, **positive edge**-triggered flip-flops are used, so the data on the **D inputs** are stored **simultaneously** by the flip-flops on the **positive edge** of the clock, as indicated in the timing diagram in Figure 1.19 (b).







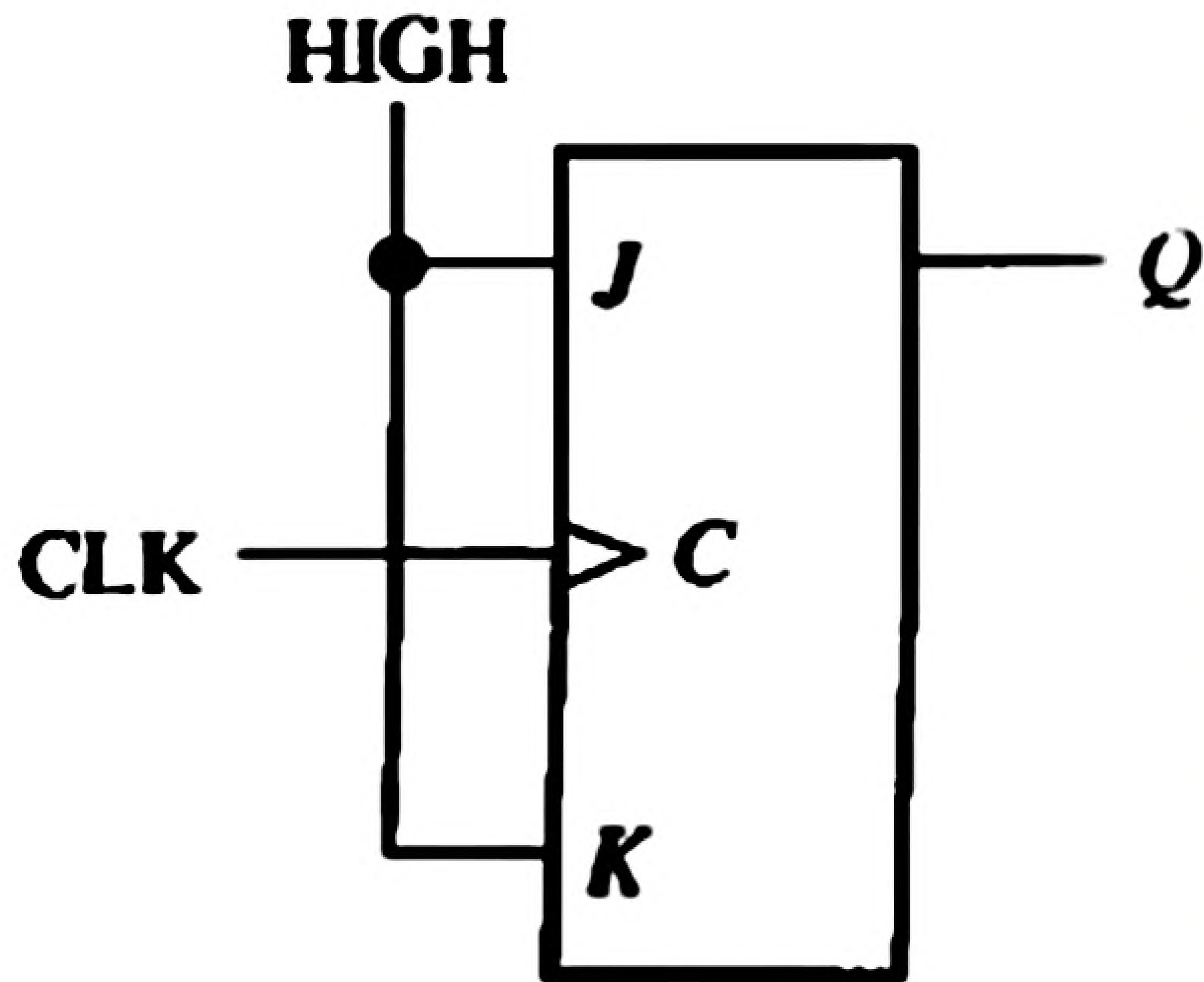
- ✓ Also, the **asynchronous reset** (R) inputs are **connected** to a common CLR line, which initially **resets** all the flip-flops.
- ✓ This **group** of **four** flip-flops is an example of a **basic register** used for **data** storage.
- ✓ In **digital systems**, data are normally **stored** in **groups** of bits (usually **eight** or **multiples** thereof) that represent numbers, codes, or other information.



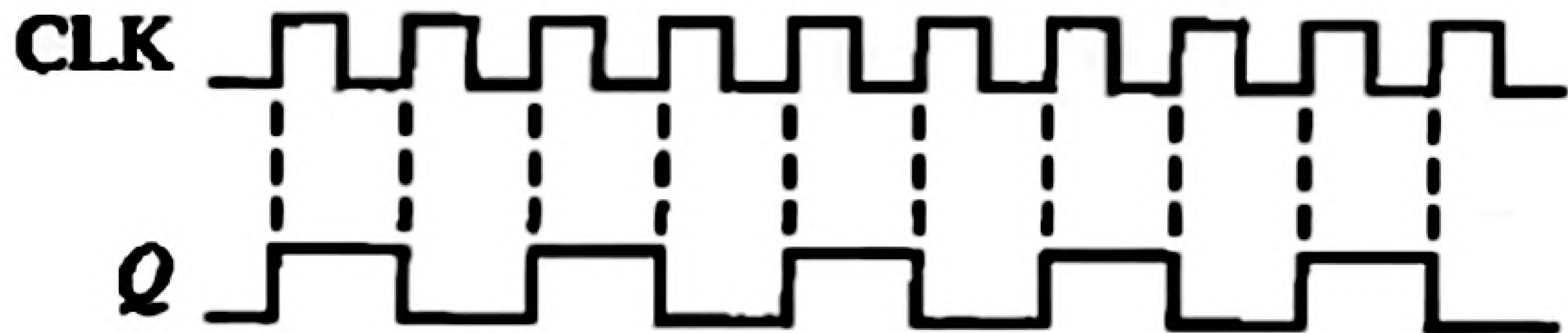
### 1.11.2- Frequency Division.

- ✓ **Another application** of a flip-flop is **dividing** (**reducing**) the frequency of a periodic waveform.
- ✓ When a **pulse waveform** is applied to the clock input of a J-K flip-flop that is **connected** to **toggle** ( $J = K = 1$ ), the Q output is a **square wave** with **one-half** the frequency of the clock input.
- ✓ Thus, a **single flip-flop** can be applied as a **divide-by-2** device, as is illustrated in **Figure 1.20**.







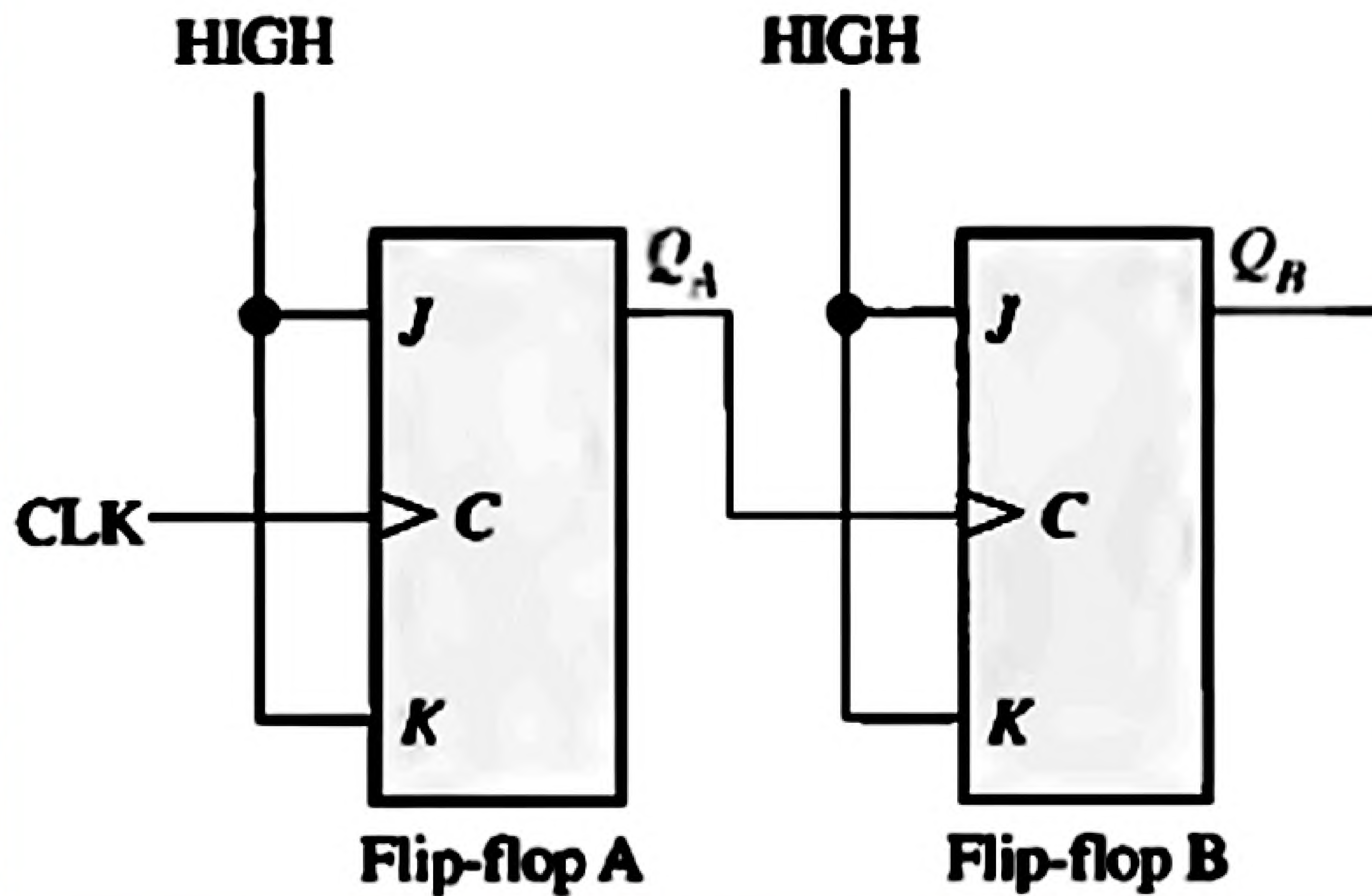


**Figure 1.20** The J-K flip-flop as a divide-by-2 device. Q is one-half the frequency of CLK.



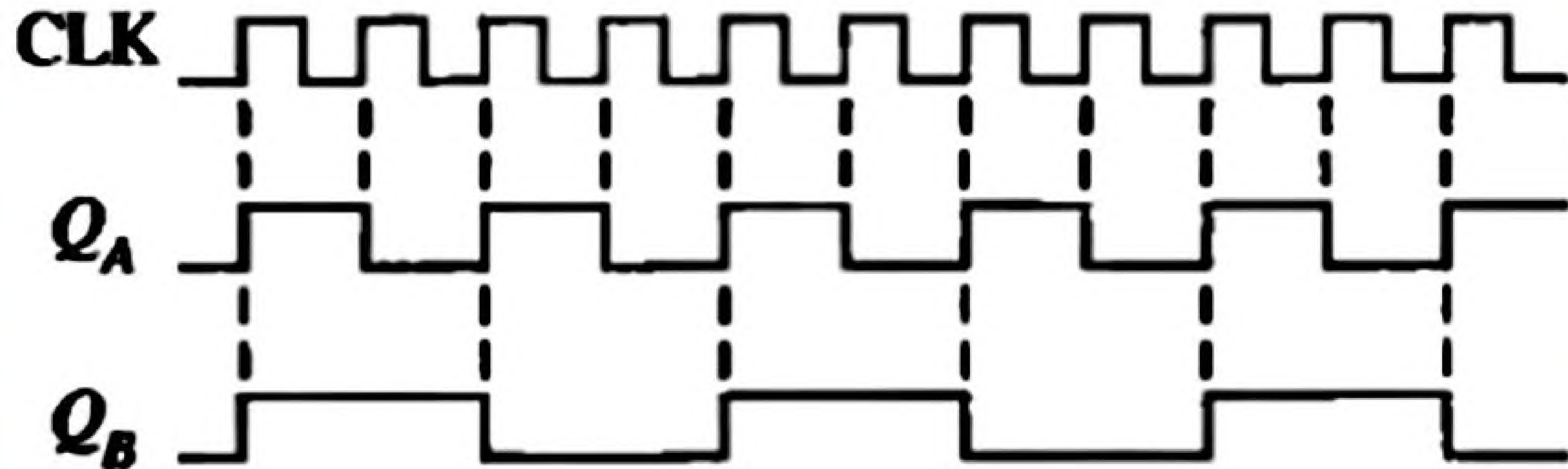
- ✓ As you can see, the **flip-flop** changes state on **each triggering** clock edge (**positive edge**-triggered in this case).
- ✓ This results in an **output** that **changes** at **half** the **frequency** of the clock waveform.
- ✓ Further **division** of a **clock frequency** can be **achieved** by using the output of one flip-flop **as the clock** input to a **second** flip-flop, as shown in Figure 1.21.





(a)





(b)

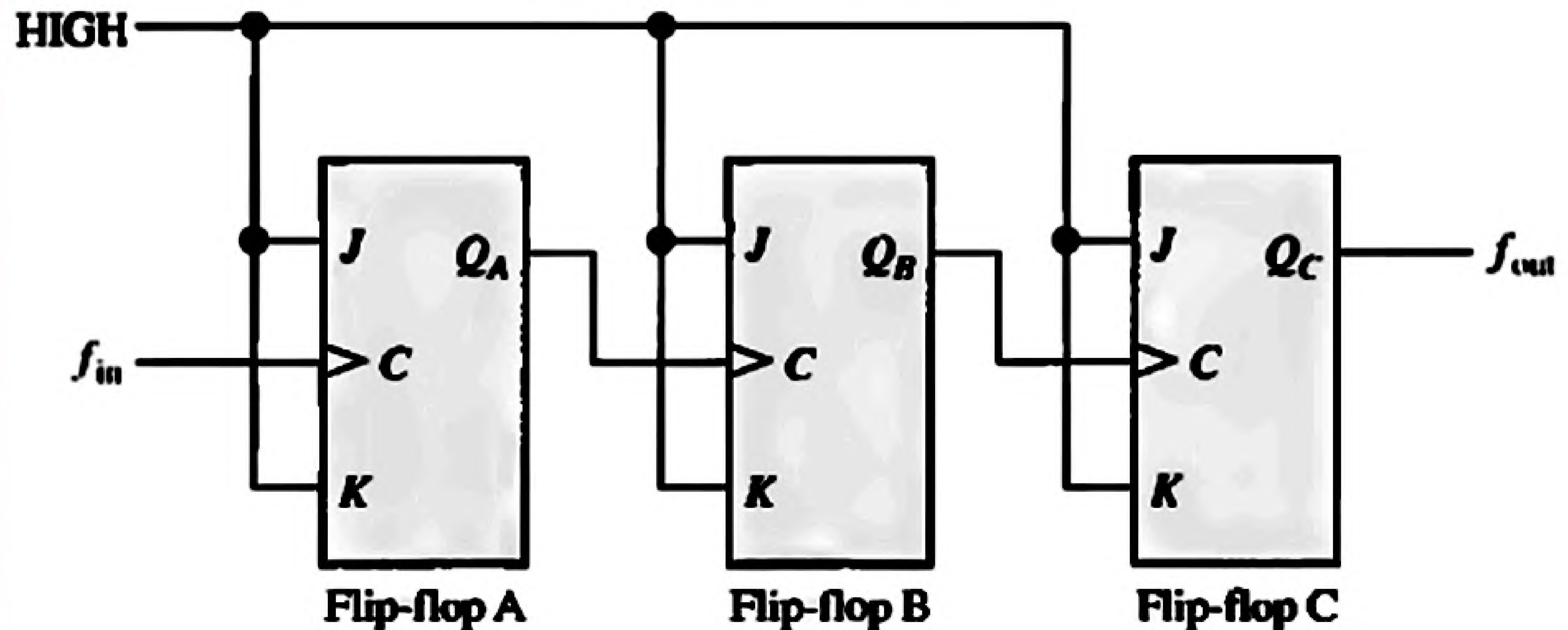
**Figure 1.21** Example of **two** J-K flip-flops used to **divide** the **clock** frequency by 4.  $Q_A$  is **one-half** and  $Q_B$  is **one-fourth** the frequency of CLK.



- ✓ The **frequency** of the  $Q_A$  **output** is **divided** by 2 by flip-flop B.
- ✓ The  $Q_B$  **output** is, therefore, **one-fourth** the frequency of the **original clock** input. **Propagation** delay times are not shown on the **timing** diagrams.
- ✓ By **connecting** flip-flops in this way, a **frequency division** of  $2^n$  is achieved, where **n** is the **number** of flip-flops.
- ✓ For example, **three flip**-flops divide the clock frequency by  $2^3 = 8$ ; **four** flip-flops divide the clock frequency by  $2^4 = 16$ ; and so on.



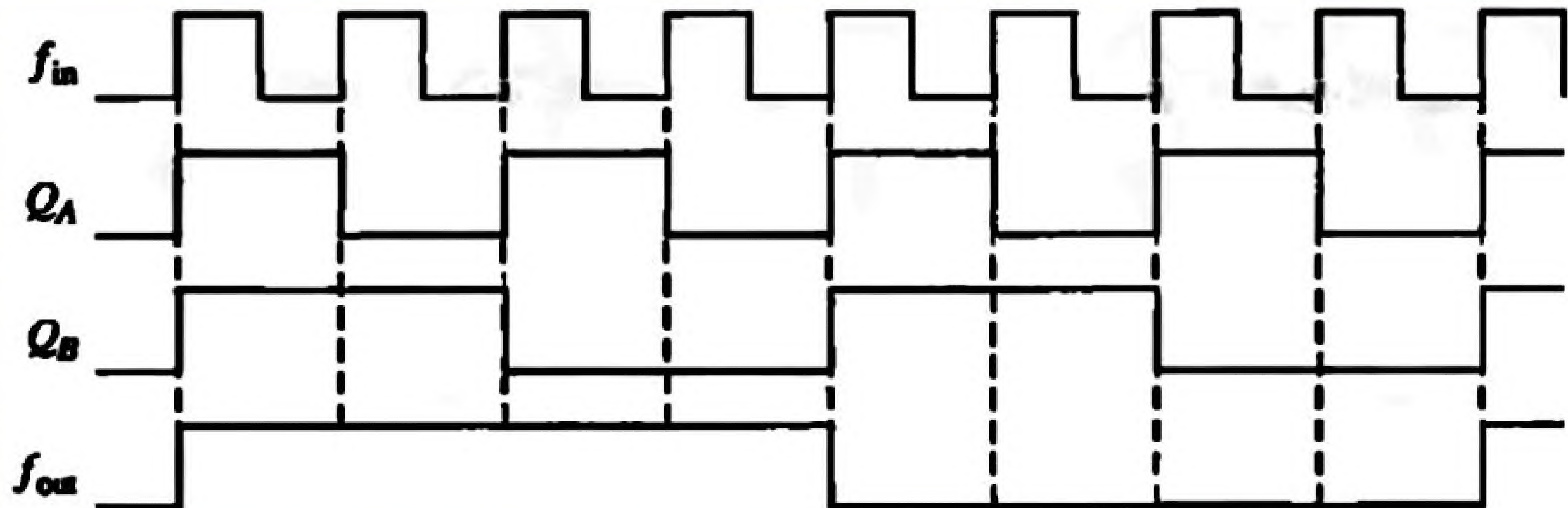
**Example 1.9:** Develop the  $f_{out}$  waveform for the circuit in the Figure, when an **8 kHz square** wave input is applied to the clock input of flip-flop A.





### Solution:

- ✓ The **three flip-flops** are connected to divide the input frequency by eight ( $2^3 = 8$ ) and the  **$f_{out}$**  waveform is shown in the Figure.



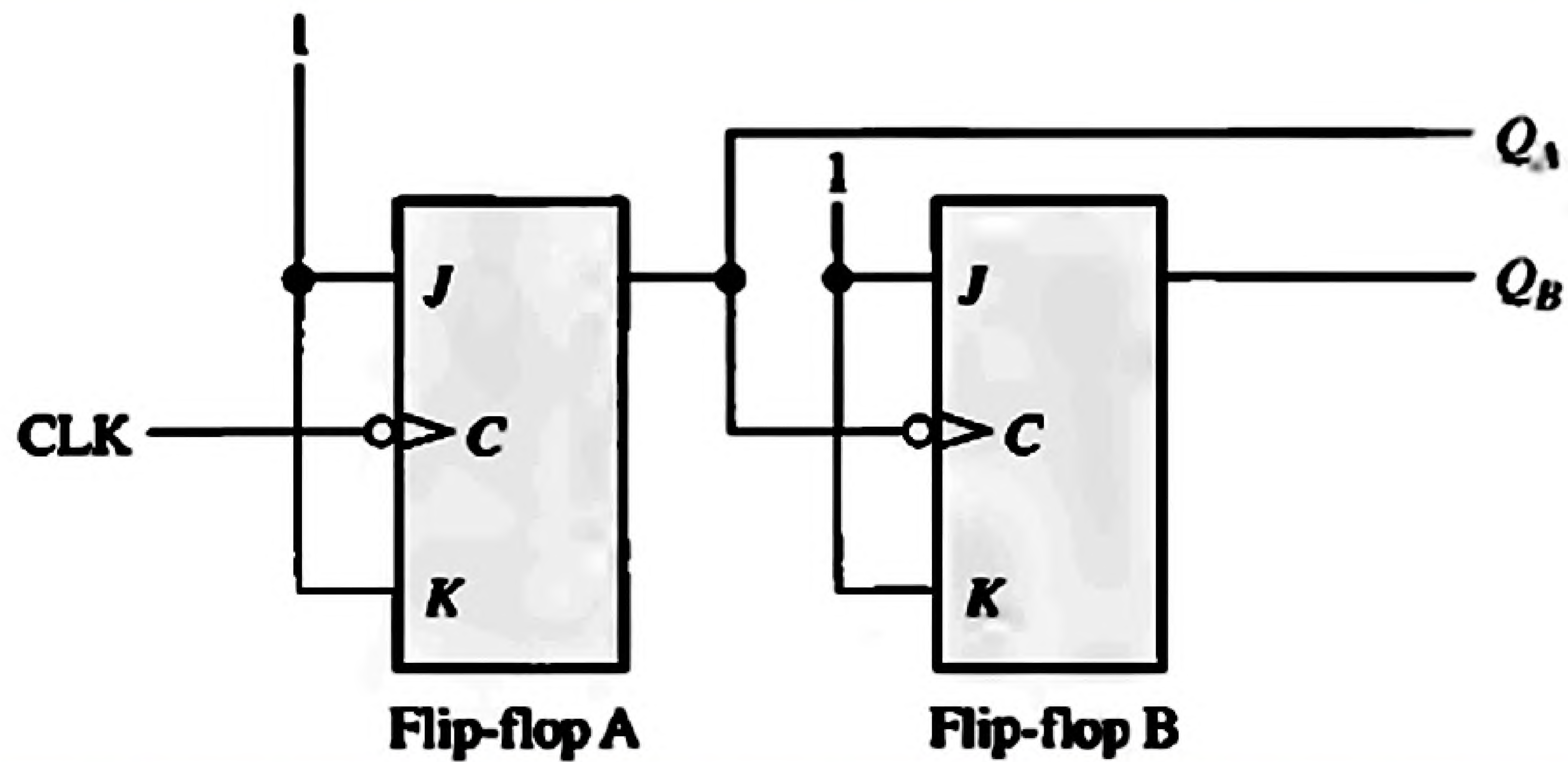


- ✓ Since these are **positive edge**-triggered flip-flops, the **outputs change** on the **positive**-going clock edge.
- ✓ There is **one output** pulse for every **eight input** pulses, so the **output frequency** is 1 kHz. Waveforms of  $Q_A$  and  $Q_B$  are also shown.

### 1.11.3- Counting.

- ✓ **Another important** application of flip-flops is in **digital counters**, which are covered in detail in **Chapter 2**. The concept is illustrated in Figure 1.22.



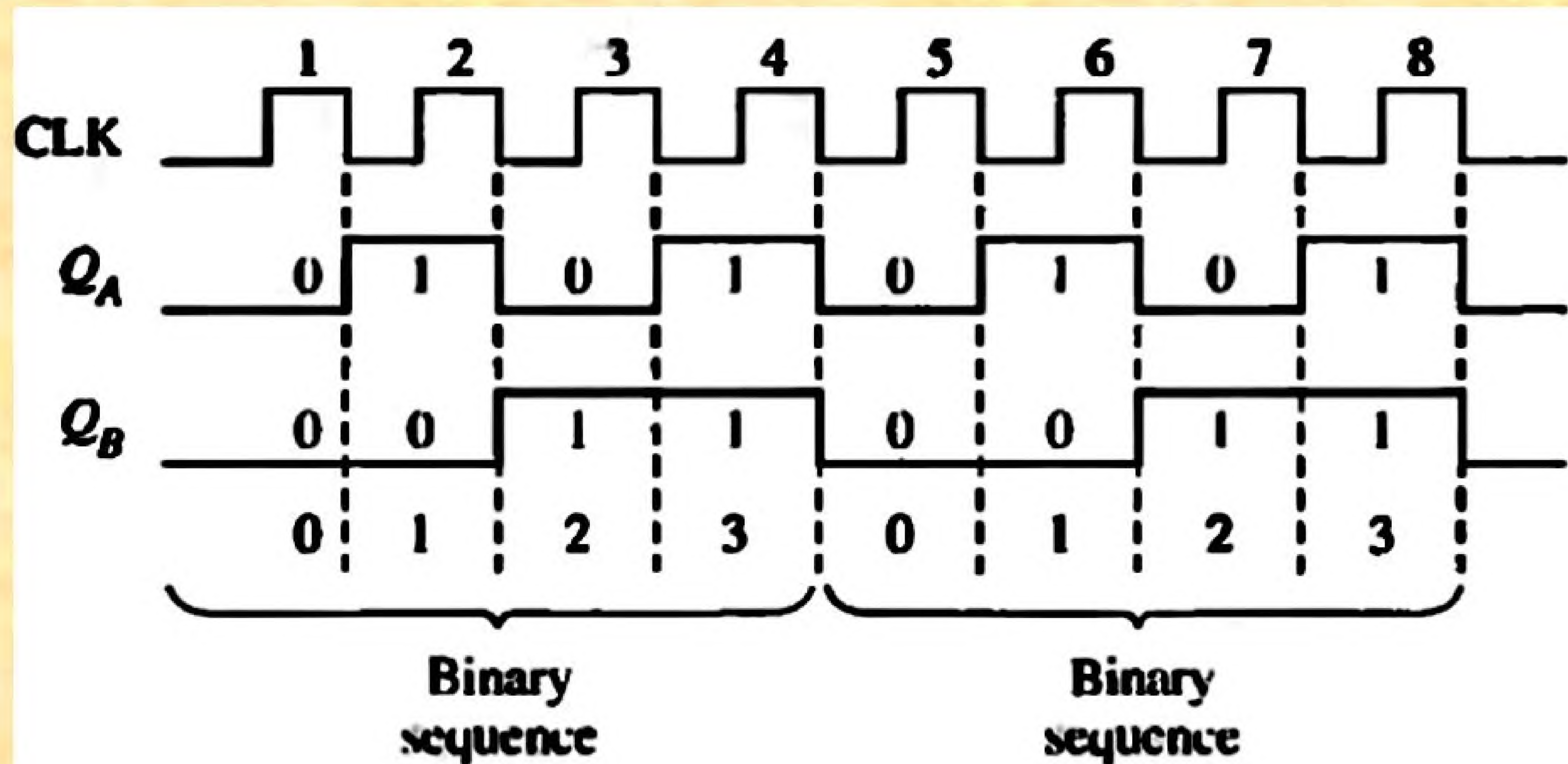




- ✓ The **flip-flops** are **negative** edge-triggered J-Ks. Both flip-flops are **initially RESET**.
- ✓ **Flip-flop A toggles** on the **negative**-going transition of each clock pulse.
- ✓ The **Q output** of flip-flop A **clocks** flip-flop B, so each time  $Q_A$  makes a **HIGH-to-LOW** transition, flip-flop B toggles.



- ✓ The **resulting**  $Q_A$  and  $Q_B$  waveforms are shown in the Figure. **Observe** the sequence of  $Q_A$  and  $Q_B$  in Figure 1-22.





- ✓ **Prior** to **clock** pulse 1,  $Q_A = 0$  and  $Q_B = 0$ ; after clock pulse 1,  $Q_A = 1$  and  $Q_B = 0$ ; after clock pulse 2,  $Q_A = 0$  and  $Q_B = 1$ ; and after clock pulse 3,  $Q_A = 1$  and  $Q_B = 1$ .
- ✓ If we take  $Q_A$  as the **least significant** bit, a **2-bit** sequence is produced as the flip-flops are clocked.
- ✓ This **binary sequence** repeats every **four clock** pulses, as shown in the timing diagram of Figure 1.22.
- ✓ Thus, the **flip-flops** are **counting** in sequence from **0 to 3** (00, 01, 10, 11) and then **recycling** back to 0 to begin the sequence again.



**Example 1:10:** Determine the output waveforms in relation to the clock for  $Q_A$ ,  $Q_B$  and  $Q_C$  in the circuit shown in the Figure 1.23 (a), and show the binary sequence represented by these waveforms.

**Solution:**

- ✓ The **output timing** diagram is shown in Figure 1.23 (b).
- ✓ Notice that **the outputs** change on the **negative-going** edge of the clock pulses.
- ✓ The **outputs** go through the **binary** sequence **000**, **001**, **010**, **011**, **100**, **101**, **110**, and **111** as indicated.



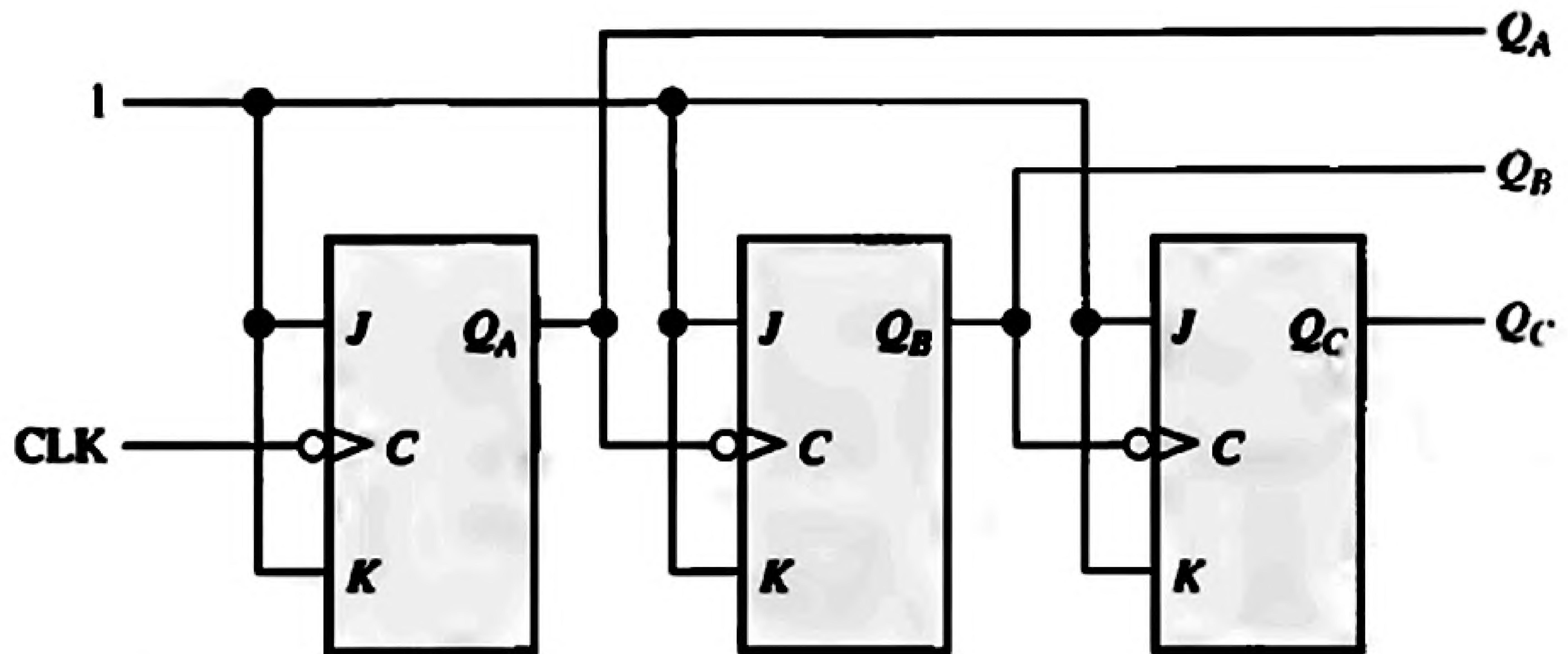
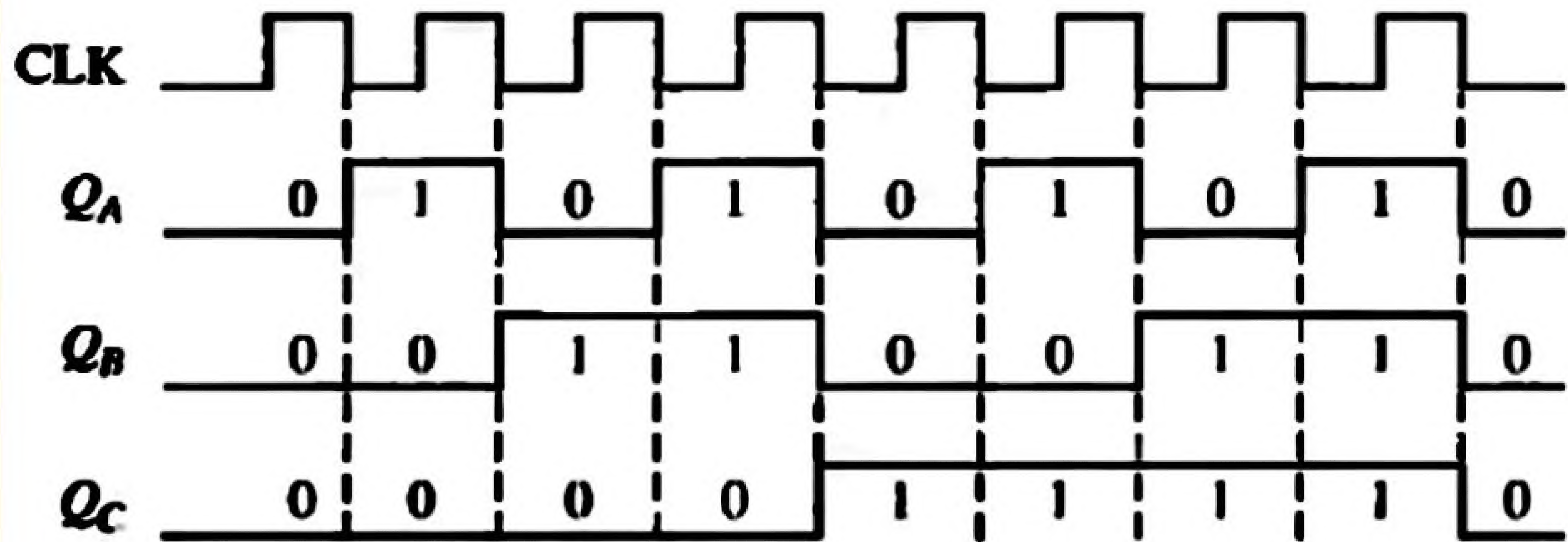


Figure 1.23 (a)





**Figure 1.23 (b)**